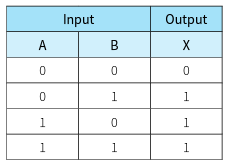
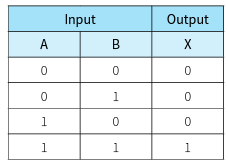
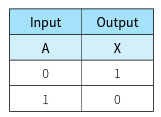
**Chapter 4 logic gate review**

**4.1 types of logic gate**

(1) AND gate (2) OR gate (3) NOT gate



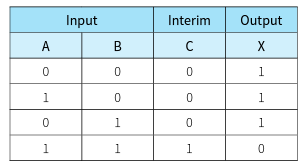
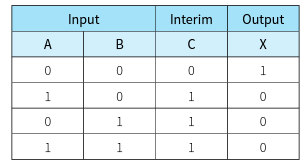
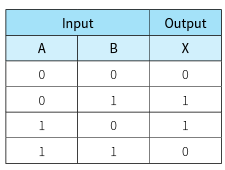
If A and B are both 1 then X will be 1. If A or B is 1 then X will be 1 The input and output are on the contrary



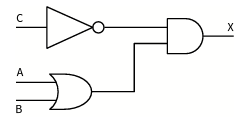
(4) NAND gate (5) NOR gate (6) XOR gate



If A and B are both 1 then X will be 0. If A or B is 1 then X will be 0. If A and B are the same then X will be 0

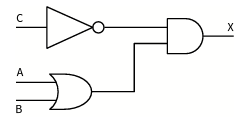


**3.2 logic circuits**

4.2 Trace table

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

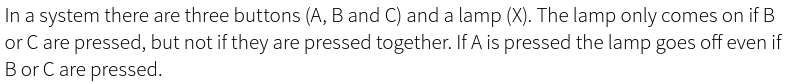
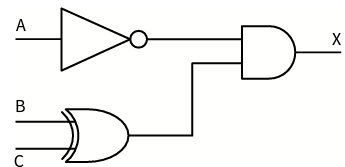
**4.3 creating a circuit diagram from a logic statement**



X= (NOT C) AND (A OR B)

X=C’·(A+B)

**4.4 creating a logic circuit to solve a problem**



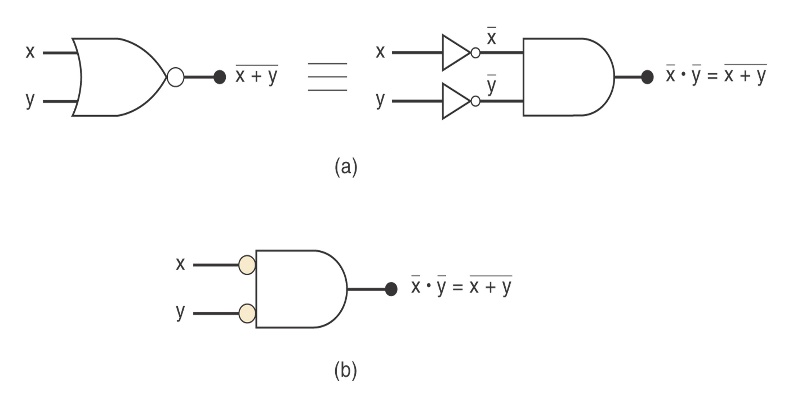
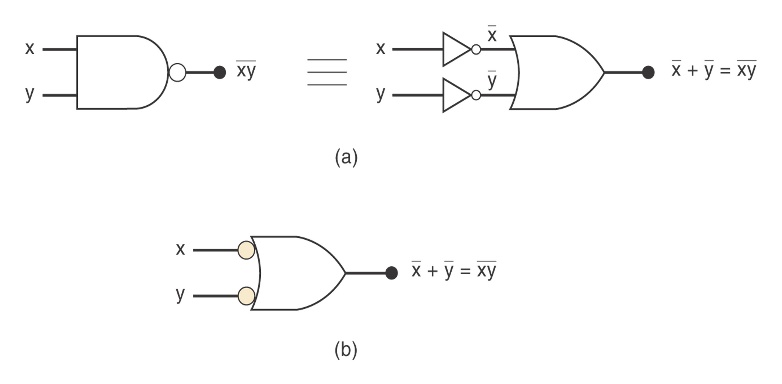
The logic statement would be X =(NOT A ) AND (B XOR C)

Logic circuit:

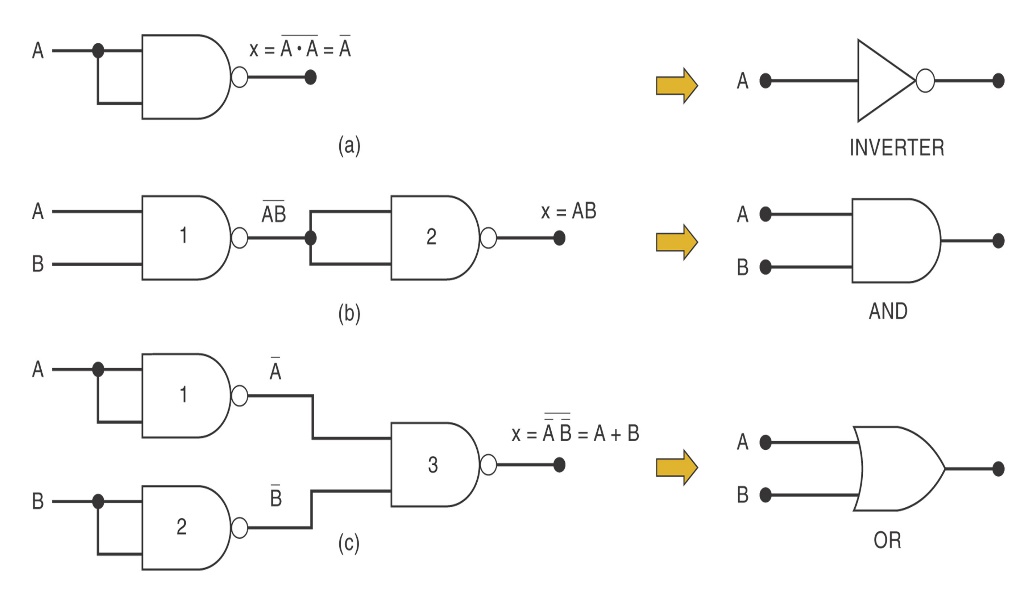
* 1. DeMorgan’s Theorems

(x+y)’=x’y’ (xy)’=x’+y’

Implications and alternative symbol for NOR function Implications and alternative symbol for NAND function

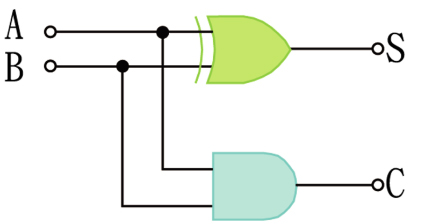
 

4.6 Universality of NAND Gates



4.7 Half adder

A half adder calculates the sum and stores the value of the carry bit c as well as the result s.



Truth table

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **s** |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |